REMARKS

After entry of this amendment, claims 33-40 and 48-61 will be pending in this application. Claims 33, 48, and 52 have been amended. Claims 41-47 have been canceled without prejudice. New claims 55-61 have been added. Support for the new and amended claims can be found in the specification. No new matter has been added.

Claims 33-40 and 48-54 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-48 of United States patent number 6,239,613. Claims 33-40 and 48-54 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Goetting et al., United States patent number 5,365,125. Claims 33-40 and 48-54 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tavana et al., United States patent number 5,682,107. Reconsideration of the rejections and allowance of the pending claims in light of the amendments and these remarks is respectfully requested.

Double Patenting Rejection

Claims 33-40 and 48-54 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-48 of United States patent number 6,239,613. Applicants request that this rejection be held in abeyance until allowable subject matter has been indicated.

Claim 33

Claim 33 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Goetting et al. But Goetting et al. do not teach each and every element of claim 33. For example, claim 33, as amended, recites "a first tristate driver having...an output directly connected to the interconnect line...and...a second tristate driver having...an output directly connected to the interconnect line." Goetting et al. do not disclose this element.

Figures 3, 4, and 20 of Goetting et al. are cited as teaching each and every element of claim 33. (See office action mailed January 24, 2002, page 2, third paragraph.)

Figure 3 shows a logic cell including a tristate output driver stage 340 having an output line "X." (See Goetting et al., column 6, lines 9-12.) Figure 4 illustrates an arrangement of 8 of these logic cells along with their interconnect lines. Figure 27 shows this arrangement in greater detail. Though Figure 27 does not use the label "X" for any interconnect line, applicants' best understanding is that the logic cell output lines are labeled O1 through O8.

As can be seen from, for example, Figure 27A and 27F, lines O1_N and O2_N are separate vertical lines. These vertical lines connect to horizontal lines through antifuses (see Goetting et al., column 20, lines 24-32.), that is, they are not connected directly to the same interconnect line. Accordingly, Goetting et al. do not provide a first tristate driver having an output directly connected to the interconnect line and a second tristate driver having an output directly connected to the interconnect line as required by the claim.

Claim 33 also stands rejected under 35 U.S.C. § 102(b) as being anticipated by Tavana et al. But Tavana et al. do not disclose this limitation either.

Figures 3A and 4A-4C are cited as teaching each and every element of claim 33. (See office action mailed January 24, 2002, page 2, last paragraph.) For example, tristate buffers B4-B7 in Figure 4B, which correspond to 302 in Figure 3A (See Tavana et al., column 9, lines 55 and 56.) are apparently cited as teaching a first tristate driver and a second tristate driver.

But the outputs of these drivers, as in Goetting et al., connect to separate lines TQ4-TQ7. As shown in Figure 6, these lines enter a programmable routing matrix where they may drive other lines through a programmable interconnection point (PIP) that operates in one direction. (Tavana et al., column 14, lines 50-60.) Accordingly, Tavana et al. do not provide a first tristate driver having an output directly connected to the interconnect line and a second tristate driver having an output directly connected to the interconnect line as required by the claim.

For at least these reasons, claim 33 should be allowed.

Claim 48

Claim 48 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Goetting et al. But Goetting et al. do not teach each and every element of claim 48. For example, claim 48, as amended, recites "tristate control logic having outputs coupled only to the plurality of tristate devices to dynamically enable and dynamically tristate the plurality of tristate devices." Goetting et al. do not teach this limitation.

Goetting et al. provide different ways of tristating the output stage of the logic cell of Figure 3. For example, it may be tristated by global control signal ISOB. But ISOB is used for electrical isolation to protect the output devices of output stage 340 during anitfuse programming. (See Goetting et al., column 13, lines 3-22.) Also, as shown in Figure 18A, an input QOE may be used to tristate the output driver. But QOE is a programmed bit from a configuration control unit. (See Goetting et al., column 16, lines 18-20.) As such it is changed by reprogramming (see Goetting et al., column 18, lines 30-58). Thus, neither the use of ISOB or QOE teach a way to dynamically enable and dynamically tristate the plurality of tristate devices as required by the claim.

Also, the output driver of the logic cell of Figure 20C may be tristated by another logic cell. But this logic cell may be coupled to other logic cells. Thus, Goetting et al., do not provide tristate control logic having outputs coupled only to the plurality of tristate devices to dynamically enable and dynamically tristate the plurality of tristate devices as required by the claim.

Claim 48 also stands rejected under 35 U.S.C. § 102(b) as being anticipated by Tavana et al. But Tavana et al. do not teach this limitation.

Figure 3A of Tavana et al. shows tristate gates 302 having two inputs, ENLL and TS. TS may be programmably coupled to a configurable logic unit, but that configurable logic unit may also be coupled to other configurable logic units. Also, ENLL is active during configuration and reconfiguration "to prevent contention which could result if various TS lines [switch] unpredictably during configuration." (See Tavana et al., column 10, lines 9-15.) Thus, Tavana et al., do not provide tristate control

logic having outputs coupled only to the plurality of tristate devices to dynamically enable and dynamically tristate the plurality of tristate devices as required by the claim.

For at least these reasons, claim 48 should be allowed.

Other Claims

Claims 34-40 depend on claim 33, and should be allowed for at least the same reasons as claim 33, and for the additional limitations they recite.

Claims 49-51 depend on claim 48, and should be allowed for at least the same reasons as claim 48, and for the additional limitations they recite.

Claim 52 should be allowed for at least similar reasons as claim 33, and for the additional limitations it recites.

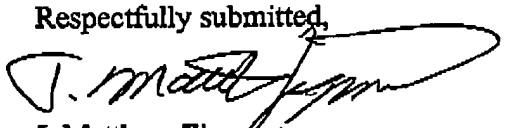
Claims 53 and 54 depend on claim 52, and should be allowed for at least the same reasons as claim 52, and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-752-2456.

Respectfully submitted,



J. Matthew Zigmant
Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
JMZ
PA 3237921 v1

VERSION WITH MARKINGS TO SHOW CHANGES MADE

33. (Amended) A method of multiplexing signals onto an interconnect line comprising:

enabling a first tristate driver having an input coupled to a first logic element and an output **[coupled]** directly connected to the interconnect line, such that a first signal is driven from the first logic element onto the interconnect line using the first tristate driver;

dynamically tristating the first tristate driver; and

dynamically enabling a second tristate driver having an input coupled to a second logic element and an output **[coupled]** directly connected to the interconnect line, such that a second signal is driven from the second logic element onto the interconnect line using the second tristate driver.

48. (Amended) A programmable logic integrated circuit comprising:

a programmable interconnect bus;

a plurality of logic elements configurable to perform logical functions;

a plurality of tristate devices coupled between the plurality of logic elements and the programmable interconnect bus;

a plurality of programmable memory cells coupled to the plurality of tristate devices to programmably enable and programmably tristate the plurality of tristate devices; and

tristate control logic having outputs coupled only to the plurality of tristate devices to dynamically enable and dynamically tristate the plurality of tristate devices.

52. (Amended) A programmable logic integrated circuit comprising:

a first logic element having a first output;

a first tristate driver having a first enable input, a second enable input, a second output, and **[an]** a first input coupled to the first output;

a first programmable memory cell coupled to the first enable input;

a second logic element coupled to the second enable input;

a third logic element having a third output;

a second tristate driver having a third enable input, a fourth output, and a second input coupled to the third output;

a second programmable memory cell coupled to the third enable input; and

an interconnect line coupled to the second output and the fourth output,

wherein the interconnect line is not coupled to the second input and the fourth input by a programmable connection, and the second logic element may dynamically tristate and dynamically enable the tristate driver.